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EXAMINER	
NGUYEN, PHU K	

ART UNIT	PAPER NUMBER
2671	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/037,992	COLLODI, DAVID
	Examiner	Art Unit
	Phu K. Nguyen	2671

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over HO et al. (WO 95/06298).

As per claim 1, Ho teaches the claimed "graphics processing unit for use in a system for lighting a plurality of polygon surfaces in a rendering system" (Ho, figure 2), the graphics processing unit comprising: a. dedicated hardware logic operable to perform a sequence of lighting calculations that generate lighting equation lighting coefficients for a plurality of the drawn pixels (Ho, TreflectanceShader, page 16, lines 24-24; page 18, lines 1-4; page 19, lines 3-8); and b. user programmable hardware logic communicating with the dedicated hardware logic to receive the lighting coefficients and perform additional shading calculations using the lighting coefficients (Ho, e.g., TimageMapShader, page 24, lines 33-36; TprocedureMapShader, page 26, lines 27-29; ...). It is noted that Ho does not explicitly teach the characteristic of the system as "per-pixel" as claimed. However, Ho's shading evaluation performs calculation at each vertex pixels and interpolates the remaining pixels suggests the property of system as "per-pixel" as claimed. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to configure H's system as claimed because the process "per-pixel" of the system will enhance the quality of the visual representation of the object on the screen.

Claim 2 adds into claim 1 “the dedicated hardware logic communicates with the programmable hardware logic through one or more shared registers” which would have been obvious because the use of common shared registers improves the simplification of the hardware and reduces the cost to build.

Claim 3 adds into claim 1 “the dedicated hardware logic comprises logic that uses the lighting coefficients in the calculation of a color value” which H teaches in page 19, lines 3-13.

Claim 4 adds into claim 1 “the dedicated hardware logic includes a vector generation unit that receives vertex values for the polygon surfaces and calculates a 3-dimensional, unit-length surface normal vector” which Ho teaches in page 17, line 16 (e.g., surface normal N).

Claim 5 adds into claim 4 “the vector generation unit calculates a 3-dimensional, unit-length view reflection vector” which Ho teaches in page 17, line 19 (Light Reflection vector R).

Claim 6 adds into claim 1 “the dedicated hardware logic includes a point light unit that calculates normalized point light vectors” which Ho teaches in page 17, line 17 (Light vector L)

Claim 7 adds into claim 6 "the point light unit calculates scalar distance coefficients" which Ho teaches in page 17, lines 14-15 (Light attenuation factor).

Claim 8 adds into claim 1 "the dedicated hardware logic includes a vector shading unit that performs vector dot product operations" which would have been obvious in Phong's illumination model (Ho, page 18, lines 1-4) because in that model, the dot products between the light vector, camera vector, and surface normal have been used to calculate the Reflection values to enhance the shaded object.

Claim 9 adds into claim 8 "the vector shading unit performs color scaling operations" which Ho teaches in page 19, lines 3-11 (e.g., ObjectColor).

Claim 10 adds into claim 4 "the vector generation unit receives a bump map vector and combines the bump map vector with the normal vector to produce a composite surface angle vector" which Ho teaches in page 20, lines 32-36 (TbumpMap).

Claim 11 adds into claim 4 "the vector shading unit receives eye vector information" which Ho teaches in page 17, lines 20-21 (Camera vector). It would have been obvious to "generate a view reflection vector" from the viewing vector because the reflection light must be depend upon the viewing angle or vector for naturally

representing the realistic model.

Claim 12 adds into claim 11 "a texture memory communication with the programmable hardware logic" which Ho teaches in RAM 22 (figure 2; page 19, lines 25-30).

As per claim 13, Ho teaches the claimed "graphics processing unit for use in a system for lighting a plurality of polygon surfaces in a rendering system" (Ho, figure 2), the graphics processing unit comprising: a. dedicated hardware logic operable to perform a sequence of lighting calculations that generate specular lighting value coefficients for a plurality of the drawn pixels (Ho, TreflectanceShader, page 16, lines 24-24; page 18, lines 1-4; page 19, lines 3-8); and b. per-pixel user programmable hardware logic communicating with the dedicated hardware logic to receive the lighting coefficients and perform additional shading calculations using the specular lighting value coefficients (Ho, e.g., TimageMapShader, page 24, lines 33-36; TprocedureMapShader, page 26, lines 27-29; ...). It is noted that Ho does not explicitly teach the characteristic of the system as "per-pixel" as claimed. However, Ho's shading evaluation performs calculation at each vertex pixels and interpolates the remaining pixels suggests the property of system as "per-pixel" as claimed. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to configure H's system as claimed because the process "per-pixel" of the system will enhance the quality of the visual representation of the object on the screen.

Claim 14 adds into claim 13 “the dedicated hardware logic communicates with the programmable hardware logic through one or more shared registers” which would have been obvious because the use of common shared registers improves the simplification of the hardware and reduces the cost to build.

Claim 15 adds into claim 13 “the dedicated hardware logic comprises logic that uses the lighting coefficients in the calculation of a color value” which H teaches in page 19, lines 3-13.

Claim 16 adds into claim 13 “the dedicated hardware logic includes a vector generation unit that receives vertex values for the polygon surfaces and calculates a 3-dimensional, unit-length surface normal vector” which Ho teaches in page 17, line 16 (e.g., surface normal N).

Claim 17 adds into claim 16 “the vector generation unit calculates a 3-dimensional, unit-length view reflection vector” which Ho teaches in page 17, line 19 (Light Reflection vector R).

Claim 18 adds into claim 13 “the dedicated hardware logic includes a point light unit that calculates normalized point light vectors” which Ho teaches in page 17, line 17 (Light vector L)

Claim 19 adds into claim 18 “the point light unit calculates scalar distance coefficients” which Ho teaches in page 17, lines 14-15 (Light attenuation factor).

Claim 20 adds into claim 13 “the dedicated hardware logic includes a vector shading unit that performs vector dot product operations” which would have been obvious in Phong’s illumination model (Ho, page 18, lines 1-4) because the dot products between the light vector, camera vector, and surface normal have been used to calculate the Reflection values to enhance the shaded object.

Claim 21 adds into claim 20 “the vector shading unit performs color scaling operations” which Ho teaches in page 19, lines 3-11 (e.g., ObjectColor).

Claim 22 adds into claim 16 “the vector generation unit receives a bump map vector and combines the bump map vector with the normal vector to produce a composite surface angle vector” which Ho teaches in page 20, lines 32-36 (TbumpMap).

Claim 23 adds into claim 16 “the vector shading unit receives eye vector information” which Ho teaches in page 17, lines 20-21 (Camera vector). It would have been obvious to “generate a view reflection vector” from the viewing vector because the reflection light must be depend upon the viewing angle or vector for naturally

representing the realistic model.

Claim 24 adds into claim 13 “a texture memory communication with the programmable hardware logic” which Ho teaches in RAM 22 (figure 2; page 19, lines 25-30).

As per claim 25, Ho teaches the claimed “graphics processing unit for use in a system for lighting a plurality of polygon surfaces in a rendering system” (Ho, figure 2), the graphics processing unit comprising: a. dedicated hardware logic operable to perform a sequence of lighting calculations that generate diffuse lighting value coefficients for a plurality of the drawn pixels (Ho, TreflectanceShader, page 16, lines 24-24; page 18, lines 1-4; page 19, lines 3-8); and b. user programmable hardware logic communicating with the dedicated hardware logic to receive the lighting coefficients and perform additional shading calculations using the diffuse lighting value coefficients (Ho, e.g., TimageMapShader, page 24, lines 33-36; TprocedureMapShader, page 26, lines 27-29; ...). It is noted that Ho does not explicitly teach the characteristic of the system as “per-pixel” as claimed. However, Ho’s shading evaluation performs calculation at each vertex pixels and interpolates the remaining pixels suggests the property of system as “per-pixel” as claimed. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to configure H’s system as claimed because the process “per-pixel” of the system will enhance the quality of the visual representation of the object on the screen.

Claim 26 adds into claim 25 “the dedicated hardware logic communicates with the programmable hardware logic through one or more shared registers” which would have been obvious because the use of common shared registers improves the simplification of the hardware and reduces the cost to build.

Claim 27 adds into claim 25 “the dedicated hardware logic comprises logic that uses the lighting coefficients in the calculation of a color value” which H teaches in page 19, lines 3-13.

Claim 28 adds into claim 25 “the dedicated hardware logic includes a vector generation unit that receives vertex values for the polygon surfaces and calculates a 3-dimensional, unit-length surface normal vector” which Ho teaches in page 17, line 16 (e.g., surface normal N).

Claim 29 adds into claim 28 “the vector generation unit calculates a 3-dimensional, unit-length view reflection vector” which Ho teaches in page 17, line 19 (Light Reflection vector R).

Claim 30 adds into claim 25 “the dedicated hardware logic includes a point light unit that calculates normalized point light vectors” which Ho teaches in page 17, line 17 (Light vector L)

Claim 31 adds into claim 30 "the point light unit calculates scalar distance coefficients" which Ho teaches in page 17, lines 14-15 (Light attenuation factor).

Claim 32 adds into claim 25 "the dedicated hardware logic includes a vector shading unit that performs vector dot product operations" which would have been obvious in Phong's illumination model (Ho, page 18, lines 1-4) because the dot products between the light vector, camera vector, and surface normal have been used to calculate the Reflection values to enhance the shaded object.

Claim 33 adds into claim 32 "the vector shading unit performs color scaling operations" which Ho teaches in page 19, lines 3-11 (e.g., ObjectColor).

Claim 34 adds into claim 28 "the vector generation unit receives a bump map vector and combines the bump map vector with the normal vector to produce a composite surface angle vector" which Ho teaches in page 20, lines 32-36 (TbumpMap).

Claim 35 adds into claim 28 "the vector shading unit receives eye vector information" which Ho teaches in page 17, lines 20-21 (Camera vector). It would have been obvious to "generate a view reflection vector" from the viewing vector because the reflection light must be depend upon the viewing angle or vector for naturally

representing the realistic model.

Claim 36 adds into claim 25 "a texture memory communication with the programmable hardware logic" which Ho teaches in RAM 22 (figure 2; page 19, lines 25-30).

As per claim 37, Ho teaches the claimed "graphics processing unit for use in a system for lighting a plurality of polygon surfaces in a rendering system" (Ho, figure 2), the graphics processing unit comprising: a. dedicated hardware logic operable to perform a sequence of lighting calculations including the calculation of a substantially normalized point light vector (Ho's Light Vector L, page 17, line 17) (Ho, TreflectanceShader, page 16, lines 24-24; page 18, lines 1-4; page 19, lines 3-8); and b. user programmable hardware logic communicating with the dedicated hardware logic to receive the substantially normalized point light vector and perform additional shading calculations (Ho, e.g., TimageMapShader, page 24, lines 33-36; TprocedureMapShader, page 26, lines 27-29; ...). It is noted that Ho does not explicitly teach the characteristic of the system as "per-pixel" as claimed. However, Ho's shading evaluation performs calculation at each vertex pixels and interpolates the remaining pixels suggests the property of system as "per-pixel" as claimed. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to configure H's system as claimed because the process "per-pixel" of the system will enhance the quality of the visual representation of the object on the screen.

Claim 38 adds into claim 37 “point light data provided to the graphics processing unit” which Ho teaches in page 17, lines 25-26 (light sources).

Claim 39 adds into claim 38 “the point light data includes a surface position vector and point light position vector” which Ho teaches in page 17, lines 16-18.

Claim 40 adds into claim 38 “point light data for multiple light sources is input into the graphics processing unit in order to produce multiple normalized point light vectors” which would have been obvious in view of Ho’s special light sources (page 17, lines 25-26) because the use of multiple light sources yields a realistic representation of the scene environment.

Claim 41 adds into claim 38 “the substantially normalized point light vectors for the multiple light sources are calculated in parallel” which would have been obvious in view of Ho’s pipeline system because the parallel calculation improves the efficiency of the system and reduces the operation time.

Claim 42 adds into claim 38 “the dedicated hardware is operable to calculate a dot product” which would have been obvious in Phong’s illumination model (Ho, page 18, lines 1-4) because in this model, the dot products between the light vector, camera

vector, and surface normal have been used to calculate the Reflection values to enhance the shaded object.

Claim 43 adds into claim 38 "the substantially normalized point light vector includes a value that represents the intensity of the light at a surface point of a polygon surface" which would have been obvious in view of Ho's light vector L because the intensity of the light at the surface enhances the shading process and improves the quality of the visual representation of the object.

As per claim 44, Ho teaches the claimed "graphics processing unit for use in a system for lighting a plurality of polygon surfaces in a rendering system" (Ho, figure 2), the graphics processing unit comprising: a. dedicated hardware logic operable to perform a sequence of lighting calculations including the calculation of a surface normal vector (Ho, Surface Normal N, page 17; TreflectanceShader, page 16, lines 24-24; page 18, lines 1-4; page 19, lines 3-8); and b. user programmable hardware logic communicating with the dedicated hardware logic to receive the surface normal vector and perform additional shading calculations (Ho, e.g., TimageMapShader, page 24, lines 33-36; TprocedureMapShader, page 26, lines 27-29; ...). It is noted that Ho does not explicitly teach the characteristic of the system as "per-pixel" as claimed. However, Ho's shading evaluation performs calculation at each vertex pixels and interpolates the remaining pixels suggests the property of system as "per-pixel" as claimed. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention

was made to configure H's system as claimed because the process "per-pixel" of the system will enhance the quality of the visual representation of the object on the screen.

Claim 45 adds into claim 44 "the dedicated hardware logic communicates with the programmable hardware logic through one or more shared registers" which would have been obvious because the use of common shared registers improves the simplification of the hardware and reduces the cost to build.

Claim 46 adds into claim 45 "wherein the dedicated hardware logic includes a vector generation unit that receives vertex values for the polygon surfaces and calculates a 3-dimensional, unit-length surface normal vector" which Ho teaches in page 17, line 16 (e.g., surface normal N).

Claim 47 adds into claim 45 "the vector gėneration unit calculates a 3-dimensional, unit-length view reflection vector" which Ho teaches in page 17, line 19 (Light Reflection vector R).

As per claim 48, Ho teaches the claimed "graphics processing unit for use in a system for lighting a plurality of polygon surfaces in a rendering system" (Ho, figure 2), the graphics processing unit comprising: a. dedicated hardware logic operable to perform a sequence of lighting calculations including the calculation of a reflection vector (Ho, Light reflection Vector R, page 17; TreflectanceShader, page 16, lines 24-

24; page 18, lines 1-4; page 19, lines 3-8); and b. user programmable hardware logic communicating with the dedicated hardware logic to receive the reflection vector and perform additional shading calculations (Ho, e.g., TimageMapShader, page 24, lines 33-36; TprocedureMapShader, page 26, lines 27-29; ...). It is noted that Ho does not explicitly teach the characteristic of the system as "per-pixel" as claimed. However, Ho's shading evaluation performs calculation at each vertex pixels and interpolates the remaining pixels suggests the property of system as "per-pixel" as claimed. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to configure H's system as claimed because the process "per-pixel" of the system will enhance the quality of the visual representation of the object on the screen.

Claim 49 adds into claim 48 "the dedicated hardware logic communicates with the programmable hardware logic through one or more shared registers" which would have been obvious because the use of common shared registers improves the simplification of the hardware and reduces the cost to build.

Claim 50 adds into claim 49 "wherein the dedicated hardware logic includes a vector generation unit that receives vertex values for the polygon surfaces and calculates a 3-dimensional, unit-length surface normal vector" which Ho teaches in page 17, line 16 (e.g., surface normal N).

Claim 51 adds into claim 50 "the vector generation unit calculates a 3-

dimensional, unit-length view reflection vector" which Ho teaches in page 17, line 19 (Light Reflection vector R).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu K. Nguyen whose telephone number is (703)305 - 9796. The examiner can normally be reached on M-F 8:00-4:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu K. Nguyen
March 15, 2004